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Sub-micrometer epitaxial Josephson junctions for quantum circuits

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Abstract
We present a fabrication scheme and testing results for epitaxial sub-micrometer Josephson junctions. The junctions are made using a high-temperature (1170 K) 'via process' yielding junctions as small as 0.8 μm in diameter by use of optical lithography. Sapphire (Al_2O_3) tunnel-barriers are grown on an epitaxial Re/Ti multilayer base-electrode. We have fabricated devices with both Re and Al top-electrodes. While room temperature (295 K) resistance versus area data are favorable for both types of top-electrodes, the low-temperature (50 mK) data show that junctions with the Al top-electrode have a much higher subgap resistance. The microwave loss properties of the junctions have been measured by use of superconducting Josephson junction qubits. The results show that high subgap resistance correlates with improved qubit performance.

(Some figures may appear in colour only in the online journal)

1. Introduction

Josephson junction superconducting devices are promising candidates for qubit use in quantum information circuits [1]. The tunnel-barriers in these junctions are typically amorphous AlO_x made by room temperature ($T = 295$ K) oxidation of thin films of aluminum. Qubit spectroscopy reveals coupling to stochastically distributed two-level systems (TLS) in the tunnel-barrier [2]. These TLS are observed as avoided level crossings (i.e., splittings) in the qubit spectroscopy. For the amorphous AlO_x tunnel-barrier, the density of TLS splittings is measured to be 0.5 $(\mu m^2\ GHz)^{-1}$ [3, 4]. While the physical origin of TLS is still under debate, it is clear that their interaction with the qubit is detrimental because they can absorb energy and decohere the qubit state. These TLS have a random distribution in frequency space and coupling strength. Unless some strategy for reducing the number of TLS is used, it is highly likely that TLS splittings will appear close to the desired operation frequency when circuits with multiple qubits are constructed.

To date, there have been two strategies for reducing the number of TLS in qubit junctions. The first is to reduce the junction area as much as possible. Sub-micrometer Josephson junctions made by use of electron-beam lithography and Al shadow-evaporation [5] are highly successful in charge qubits, transmons, flux qubits, and low-impedance flux qubits [6–9]. However, the absence of metal crossovers in electron beam-defined circuits limits the available circuit designs (e.g., no gradiometric flux coils). Step-edge junctions fabricated by use of optical lithography for phase qubits can be made as small as 1 μm^2 [10, 11]. While crossovers are

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part of step-edge technology, multiple-qubit circuits will still suffer from the residual stochastic TLS splitting distribution due to the high density of TLS splittings.

The second strategy is to reduce the TLS density by use of epitaxial materials. While this typically involves high-temperature processing [12], it has yielded improved performance. Oh *et al* observed an ∼80% reduction in the density of TLS in a large area (70 μm^2) phase qubit with a crystalline Al_2O_3 tunnel-barrier when compared to amorphous AlO_x [13]. This technology uses optical lithography, and crossovers are easily made.

Our goal in this work is to combine these two strategies by developing a process for reducing the size of epitaxial junctions for high-coherence qubits. In addition, we evaluate the efficacy of replacing the Al top-electrode with Re. This is motivated by the discussion in [13], where it was hypothesized that the residual TLS may originate at the Al_2O_3–Al interface. To test this hypothesis, we studied Re top-electrode junctions and qubits, and compared them to devices with Al top-electrodes.

In order to reduce the junction size, we first tried a standard trilayer process [12] but the photoresist pillar washed away in the developer rinse for junction sizes smaller than ∼2 μm. While a trilayer process for sub-micrometer junctions does exist [14], it requires chemical–mechanical planarization and this is not available in our facility. Instead, we developed a high-temperature 'via process' similar to a scheme used for masking GaN nanowire growth [15]. As discussed below, the epitaxial base-electrode is grown on a high-quality substrate, an insulator with a via to the base-electrode is defined, and the epitaxial tunnel-barrier is then grown in the via after heating and recrystallizing the surface. We have measured both the room temperature ($T = 295$ K) and low-temperature ($T < 100$ mK) properties of these single-junction devices, and we have also fabricated qubit devices and measured their performance.

2. Substrate preparation and base-electrode growth

All of our devices were fabricated on single-crystal Al_2O_3(0001) sapphire wafers. The wafers are 76.2 mm in diameter and 0.43 mm thick. As received from the manufacturer, the surface of the substrate exhibits no lateral crystalline order when imaged by atomic force microscopy (AFM), i.e., it is amorphous. To improve the crystalline order, we heat the substrate in a tube furnace to 1370 K for 20 h in a 14:1 nitrogen-to-oxygen gas mixture at atmospheric pressure [16, 17]. After the furnace treatment, we observe atomic step terraces and lateral order. In addition, we find a correlation between the miscut angle (the angle between the dicing saw cut and the (0001) crystal plane) and the terrace size measured using AFM: even a small, 0.3° miscut limits the terraces to ∼100 nm wide, while a nominal 0.0° miscut yields ∼390 nm wide terraces. However, we found that the surface morphology of the Re base-electrode is independent of furnace treatment and miscut angle.

At first we used a 165 nm thick rhenium film for the base-electrode, deposited by use of ultrahigh-vacuum (UHV) DC sputtering [18]. The substrate temperature is held at 1170 K, the deposition rate is 3 nm min^{-1}, and the argon sputter gas pressure is 0.7 Pa. For this and all subsequent layers, we rotate the substrate during deposition to improve film thickness uniformity. The magnetron sputter guns are mounted in a sputter-up configuration at 35° off normal and 15 cm from the substrate. Using this technique, we obtain crystalline rhenium films. We find that these films are characterized by ∼100 nm diameter hexagonal islands with ∼15 nm height, as shown in figure 1(a). The root mean square (rms) roughness of the Re films is 3.2 nm, and is indicative of step-bunching and limited mobility of the Re during deposition. For comparison, a polycrystalline or crystalline Nb base-electrode suitable for high-quality Nb–Al/AlO_x–Nb Josephson junction use has roughness ≤0.5 nm [19, 20].

We found that it is possible, in order to obtain a smoother Re surface for subsequent growth of the barrier, to reduce the rms roughness of the base-electrode film while maintaining crystallinity by using a Re/Ti multilayer. In this process, we deposit a 10 nm Re layer and then cap it with 1.5 nm of Ti. Both films are UHV sputtered at 1170 K. Titanium has a lower surface free energy (1.9 J m^{-2}) than rhenium (2.2 J m^{-2}) and acts as a wetting layer, resulting in a significantly smoother surface, as shown in figures 1(a) and (c). By repeating the Re/Ti unit cell structure twelve times and then capping with a 10 nm Re top layer (i.e., $(Re/Ti)_{12}Re$), we obtain base-electrode films 150 nm thick with an rms roughness of only 0.6 nm. Line scans from the respective AFM images are shown in figures 1(b) and (d), illustrating that the multilayer film is much smoother, with fewer vertical edges, than the pure Re film. Reflection high-energy electron diffraction (RHEED) patterns (not shown) from pure Re and $(Re/Ti)_{12}Re$ films are indistinguishable, indicating that base-electrode crystallinity is not degraded by using the Re/Ti multilayer. This base-electrode surface is much more favorable for tunnel-barrier growth with a sharp metal–insulator interface [19, 21, 22].

3. The tunnel-barrier and top-electrode growth

Once the base-electrode is grown, we proceed to define the tunnel junction and top-electrode by use of the via process. This process is illustrated in figure 2. The tunnel-barrier and top-electrode are deposited after the insulator and via are defined. To accomplish this, we remove the wafer (with the epitaxial base-electrode already grown) from the UHV sputter tool. The first step of the process is shown in figure 2(a), where the $(Re/Ti)_{12}Re$ base-electrode is patterned by use of a 500 V SF_6 RIE at 2 Pa, etching all the way down to the substrate. The base-electrode is then covered with a 220 nm thick crossover insulator, either SiO_x or SiN_x, by use of plasma enhanced chemical vapor deposition at $T = 295$ K.

Vias are then etched in the insulator by use of a 240 V RIE, shown in figure 2(b). We use $CHF_3 + O_2$ at 13 Pa for the SiO_x insulator and $CF_4 + O_2$ at 2 Pa for SiN_x. This step defines the tunnel junction size and shape. This RIE has a 3:1 (5:1) selectivity in etch rate between SiO_x (SiN_x) and Re, allowing us to stop fairly effectively when we

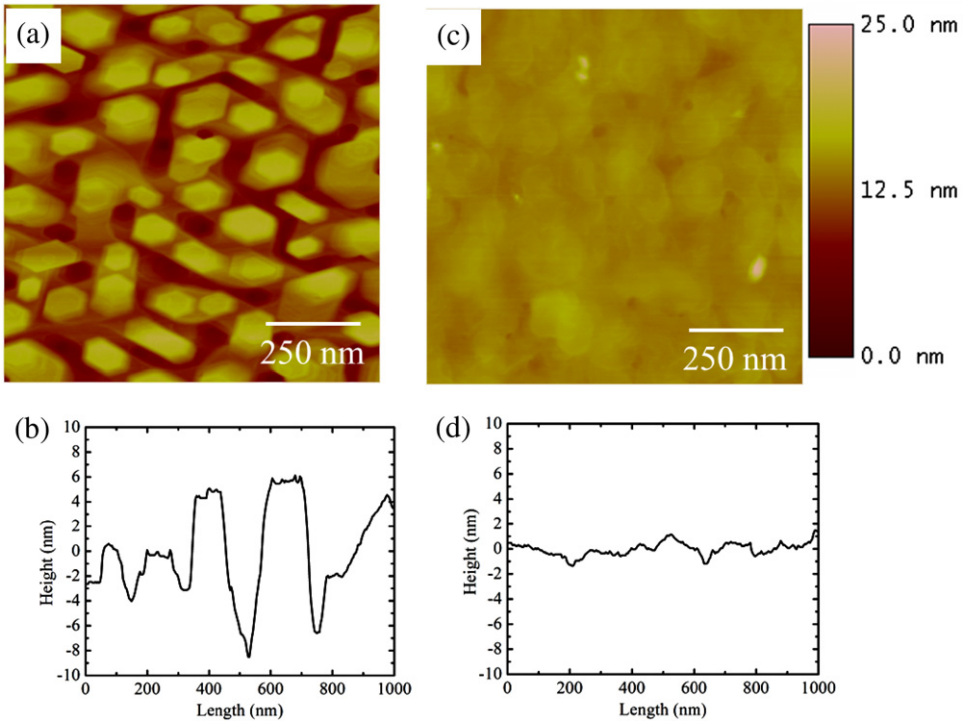

Figure 1. Comparison of base-electrode film morphology. Rhenium base-electrode 165 nm thick, sputter-deposited at 1170 K: (a) AFM image (1×1 μm^2) with rms roughness = 3.2 nm and (b) AFM line scan. $(Re/Ti)_{12}Re$ multilayer base-electrode film 150 nm thick, sputter-deposited at 1170 K: (c) AFM image (1×1 μm^2) with rms roughness = 0.6 nm and (d) AFM line scan. The *Z*-scale is 25 nm for both images.

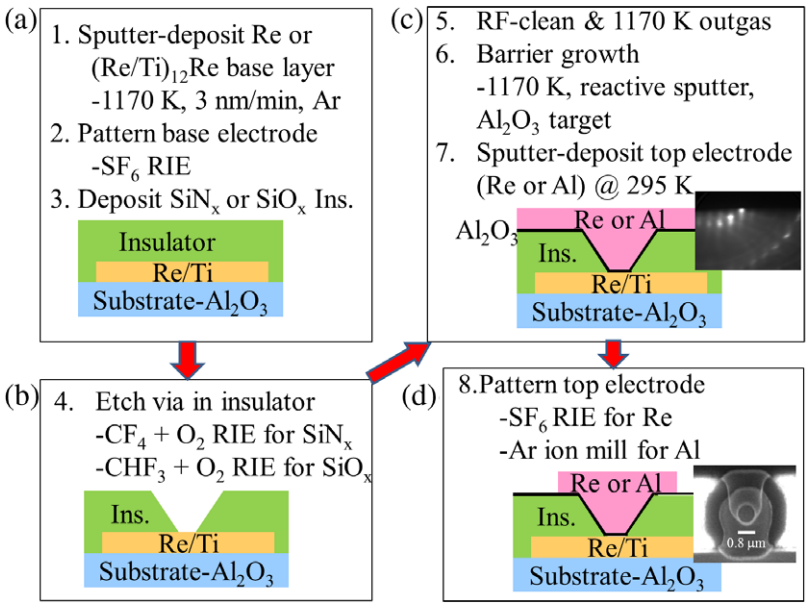

Figure 2. Fabrication schematic of epitaxial Josephson junctions. (a) The $(Re/Ti)_{12}Re$ base-electrode is patterned and encapsulated with insulator. (b) The via is etched into the insulator. (c) RF-clean, 1170 K outgas, tunnel-barrier growth, and top-electrode deposition procedures are all performed in UHV without breaking the vacuum. The inset shows a crystalline RHEED pattern of a Re base-electrode after a 1170 K anneal. (d) The top-electrode is patterned. The inset shows an SEM image of a junction with a 0.5 μm designed diameter (measured diameter = 0.8 μm). Additional wiring layers are needed for gradiometric devices.

reach the top of the crystalline Re base-electrode. Minimizing the over-etch into the base-electrode is critical, as it could create vertical walls around the edge of the via and it also could etch down to the Ti wetting layer. Tunnel-barrier coverage on these vertical sidewalls would be problematic and prone to pinholes and uneven coverage. We use a laser interferometer endpoint-detection scheme to minimize the over-etch (typically $<$10% of the total etch time). We estimate

the maximum amount of Re removed by the via over-etch and RF-clean (see below) is ∼5 nm. This leaves ∼5 nm of Re covering the nearest Ti wetting layer, so our tunnel-barriers are grown on Re, not Ti. This assertion is also confirmed by RHEED patterns: Re and Ti have distinct patterns.

After the via etch, the base-electrode in the bottom of the via has been amorphized due to the over-etch portion of the via etch. This surface needs to be cleaned and recrystallized before a tunnel junction can be grown on it. We do this by loading the wafer back into the UHV sputter tool, performing an argon RF-clean to remove ∼2 nm of material, and then heating the wafer to 1170 K for 1 h as shown in figure 2(c). The RHEED image shown in the inset of figure 2(c) and *ex situ* AFM images (not shown) indicate that the Re surface is clean and recrystallized. The epitaxial Al_2O_3 tunnel-barrier is then grown *in situ* by use of UHV RF magnetron sputtering from a sintered Al_2O_3 sputter target [23, 24]. For this deposition, the substrate temperature is held at 1170 K, the deposition rate is 0.9 nm min^{-1}, and the sputter gas pressure is 0.7 Pa argon with 5 mPa oxygen. The oxygen gas is necessary to prevent oxygen loss from the aluminum oxide at high temperature and to obtain fully stoichiometric Al_2O_3. The thickness of the tunnel-barrier is monitored *in situ* by use of spectroscopic ellipsometry. We grow crystalline aluminum oxide films 1.8 ± 0.2 nm thick as tunnel-barriers. We find that they are conformal to the Re base-electrode, as evaluated by comparing AFM images and finding them to be indistinguishable from those of the base-electrode. In addition, we note here that other barrier growth conditions were explored, for example, growing at 1170 K without oxygen and also growth at $T = 295$ K followed by an 1170 K anneal in oxygen. These resulted in a low resistance × area product (RA-product) <400 Ω μm^2 for tunnel-barriers up to 9 nm in thickness, and the RA-product was independent of the barrier thickness. From this, we conclude that tunneling was not the dominant transport mechanism for barriers grown without oxygen or at $T = 295$ K with an anneal. According to AFM and electrical isolation measurements on metallic crossovers, the SiO_x and SiN_x crossover insulators are stable (i.e., no flowing of insulator material) and isolate well even after the 1170 K processing.

The top-electrode (either Re or Al) is then deposited *in situ* by use of UHV DC magnetron sputtering after the wafer is cooled to room temperature ($T = 295$ K) in a 5 mPa oxygen background. The Al is deposited at a rate of 3 nm min^{-1}, and the argon sputter gas pressure is 0.7 Pa. For the Re top-electrode, we use xenon sputter gas instead of argon to avoid the creation of energetic neutral sputter gas atoms, which act as an unintentional mill of the tunnel-barrier during the first few atomic layers of top-electrode deposition. This is because energetic neutrals are created when there is a large mismatch in atomic mass between the sputter gas and the target material [25]. The use of xenon instead of argon for Re sputtering reduces the fractional energy of neutrals from 0.42 to 0.03. According to RHEED and AFM (not shown), the Al and Re top-electrodes exhibit moderately textured in-plane crystalline order, but small ∼30 nm grain size due to the low 295 K deposition temperature. In the final step, figure 2(d), the Re top-electrode is patterned by use of a 500 V SF_6 RIE at 2 Pa. If the top-electrode is Al, we use a 200 V argon ion mill at 0.4 Pa (oriented 20° from the substrate normal with sample rotation).

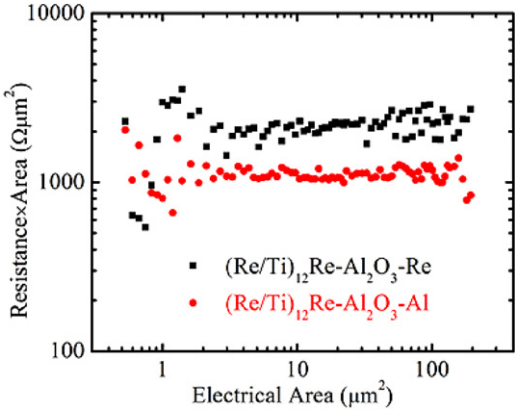

Figure 3. Room temperature ($T = 295$ K) resistance measurements of tunnel junctions with Re (black ■ curve) and Al (red • curve) top-electrodes. The resistance was measured at 100 nA bias current.

4. Electrical characterization

We measure the room temperature ($T = 295$ K) resistance of octagonal test junctions ranging in designed minimal diameter d from 0.5 to 15 μm (area: 0.2–186 μm^2). This provides three important pieces of information, including the process bias d_0. First, for medium and large junction sizes ($d \gg d_0$), the RA-product should be flat when plotted versus designed area if there are no spurious transport channels at the perimeter of the junction. Second, by plotting RA-product versus electrical area $0.827\,(d - d_0)^2$ and adjusting d_0 so that we obtain a flat RA-product curve for small junction sizes ($d \sim d_0$), we extract d_0. This gives us information concerning how the actual size of the junction differs from the designed size. Third, if the superconducting gaps of the top- and base-electrodes are known, the critical current density for the junctions in the superconducting regime can be calculated [26]. This gives us feedback for adjusting the RA-product by changing the tunnel-barrier deposition time for subsequent wafers.

Figure 3 shows a plot of RA-product versus electrical area for junctions with Re and Al top-electrodes. For both types, the curve is flat for medium and large junctions, so we expect no significant perimeter transport. Junctions of both types have a process bias of −0.3 μm, meaning that the junctions are 0.3 μm larger in diameter than designed. This agrees well with the SEM image in figure 2(d), where a junction that was designed as 0.5 μm was measured to be 0.8 μm (area = 0.5 μm^2). In order to account for the observed spread in RA-product, we designed qubit circuits with junctions of various sizes, as described in [4]. On the basis of measurements at $T = 295$ K, the top-electrodes of both types appear favorable for use as Josephson junctions.

Low-temperature ($T \sim 50$ mK) measurements were then conducted for both the Re and Al top-electrode devices in an adiabatic demagnetization refrigerator using a commercial

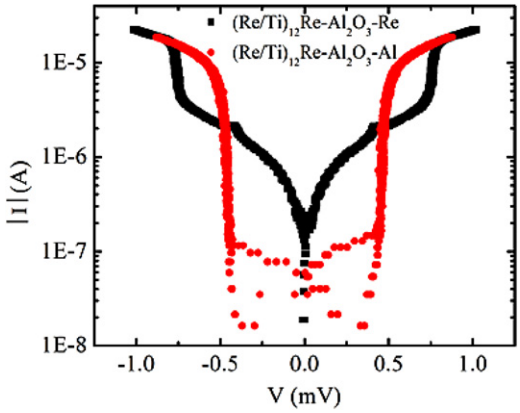

Figure 4. Low-temperature ($T \sim 50$ mK) I–V curves for the Josephson junctions with Re (black ■ curve) and Al (red • curve) top-electrodes. The superconducting branch is intentionally suppressed by a magnetic field oriented in the plane of the junction. We measure $\Delta_1 + \Delta_2 = 0.75$ meV for the junction with the Re top-electrode, and $\Delta_1 + \Delta_2 = 0.45$ meV for the junction with the Al top-electrode.

data-acquisition card and preamplifier. Figure 4 shows I–V curves for two junctions of nominally equal area ($\sim$60 μm^2) and RA-product ($\sim$2000 Ω μm^2). While the normal-state resistances, i.e., the inverse slopes of the curves above the superconducting gaps, are nearly the same, a dramatic difference in subgap structure is observed. For the Re top-electrode junction, we see low subgap resistance $R_{sg} =$ 226 Ω, indicating some transport mechanism other than pure tunneling. The subgap resistance is only five times higher than the normal-state resistance. The Al top-electrode junction shows a sharp corner, a high subgap resistance and a re-trapping current that is limited by system noise, indicative of a high-quality junction [27]. We measured tunnel junctions ranging in size from 0.5 to 186 μm^2 from five wafers with Re top-electrodes and six wafers with Al top-electrodes: all measurements exhibit the same qualitative behavior where the Re top-electrode junctions have low subgap resistance and the Al top-electrode junctions have high subgap resistance. We conclude that junctions made using Re top-electrodes have inherently poor subgap properties.

We measured the superconducting critical temperatures of the electrodes: 1.1 K (Al), 2.5 K (Re) and 2.4 K ((Re/Ti)$_{12}$Re multilayer), corresponding to superconducting gaps Δ of 0.17 meV (Al), 0.38 meV (Re) and 0.36 meV ((Re/Ti)$_{12}$Re), using BCS theory [28]. The measured values $\Delta_1 + \Delta_2$ of 0.75 meV for (Re/Ti)$_{12}$Re–Al_2O_3–Re and 0.45 meV for (Re/Ti)$_{12}$Re–Al_2O_3–Al from the I–V curves in figure 4 are in good agreement with theory.

We also measured superconducting qubits made using the via process with both Re and Al top-electrodes. We first describe a flux-biased phase qubit with an Re top-electrode. The circuit design is similar to that of [4] with qubit state measurement performed using a DC SQUID. For a device with a 4 μm^2 qubit junction with capacitance $\sim$200 fF, critical current = 2 μA, 700 fF shunt (Re/Ti)$_{12}$Re interdigitated capacitor, loop inductance $L = 720$ pH, and 1 fF SiO_x crossover insulator, we measured an energy relaxation time

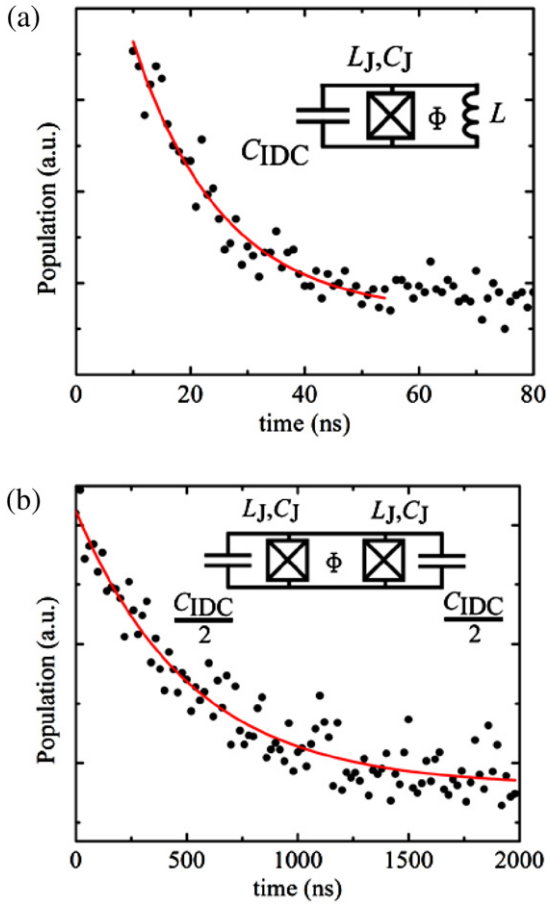

Figure 5. Low-temperature ($T < 100$ mK) energy relaxation measurements for (a) a phase qubit with an Re top-electrode: $T_1 = 15$ ns and (b) a transmon qubit with an Al top-electrode: $T_1 = 500$ ns. The solid red line is an exponential fit to data with decay time T_1. The insets show qubit circuit schematics where the Josephson junction inductance is L_J, the junction self-capacitance is C_J, and the interdigitated capacitor has capacitance C_{IDC}. The phase qubit is shunted by loop inductance L. In each case, the qubit loop is threaded by the on-chip adjustable magnetic flux Φ.

$T_1 = 15$ ns, as shown in figure 5(a). We hypothesize that T_1 is limited by the relatively low subgap resistance of the qubit junction with Re top-electrode; the classical RC decay time for the qubit is $\tau = CR_{sg} \sim 2$ ns, where $C = 900$ fF is the total qubit capacitance. We made measurements on two phase qubits from two wafers and the results yielded were similar. We were unable to detect TLS splittings in the spectroscopy data due to the broad linewidth caused by the short relaxation time of these qubits.

A qubit fabricated with an Al top-electrode showed a much longer T_1 time of 500 ns, as shown in figure 5(b). These data were taken from a transmission line shunted plasma oscillation qubit (transmon) with dispersive qubit state readout using a half-wave resonator [29]. The total qubit capacitance is given by two 1 μm^2 junctions with $\sim$100 fF capacitance (critical current = 0.1 μA), 60 fF shunt (Re/Ti)$_{12}$Re interdigitated capacitor, and 1 fF crossover SiN_x insulator. The half-wave resonator frequency is 8.3 GHz and the T_1 measurement was performed at the 7.3 GHz flux 'sweet spot'. We made measurements on two transmon qubits from

Table 1. Transmon loss analysis. The capacitance of element i is C_i, the participation ratio of element i is P_i, the loss tangent is $\tan\delta$, and the contributed loss is given by $\tan\delta \times P_i$.

Element	C_i (fF)	P_i (%)	$\tan\delta$	Contributed loss
Junction	100	62.1	3.5×10^{-5}	2.2×10^{-5}
IDC	60	37.3	4.0×10^{-5}	1.5×10^{-5}
SiN_x	1	0.6	1.0×10^{-3}	6.2×10^{-6}
			Total loss	4.3×10^{-5}

one wafer and the results yielded were similar. On the basis of the qubit resonator coupling of $g/2\pi = 85$ MHz, the qubit resonator detuning $\Delta/2\pi = 1$ GHz, and the resonator photon loss rate $\kappa/2\pi = 0.8$ MHz, the Purcell effect limit on T_1 is $(\Delta/g^2)/\kappa = 27$ μs, so our devices are not limited by the Purcell effect. We observed three TLS splittings in the spectroscopy measurement over a 0.5 GHz range (not shown), with maximum splitting size = 7 MHz.

Table 1 shows an analysis of the loss in each element of the transmon circuit: Josephson junction, interdigitated capacitor, and SiN_x insulator. The participation ratio of each element is given by $p_i = C_i/C_{\rm tot}$, where C_i is the capacitance of element i and $C_{\rm tot}$ is the total qubit capacitance. The contributed loss is given by the microwave dielectric loss tangent ($\tan\delta$) times P_i. Here we consider only the low-power loss tangent, i.e., the loss tangent measured when the TLS are unsaturated by the applied electric field [3]. We use independently measured values of $\tan\delta$ for the interdigitated capacitor and the SiN_x insulator. We use the measured $T_1 =$ 500 ns to calculate the total loss tangent of the transmon as 4.3×10^{-5} through $T_1 = 1/(2\pi f_{\rm r} \tan\delta)$, where $f_{\rm r}$ is the 7.3 GHz resonance frequency. We find that the performance of the qubit is limited primarily by loss in the Josephson junction and the interdigitated capacitor. Other loss mechanisms, such as through non-equilibrium quasiparticles, are not considered in this analysis.

5. Conclusions

We have presented a recipe for the fabrication of sub-micrometer epitaxial Josephson junctions with Al_2O_3 tunnel-barriers. The substrate crystallinity has been improved by a furnace anneal, and the base-electrode has been smoothed through the use of an $(Re/Ti)_{12}Re$ multilayer base-electrode. The epitaxial Al_2O_3 tunnel-barrier is deposited at the bottom of a via in either SiO_x or SiN_x. The top-electrodes are made from either Re or Al.

We find that Josephson junctions fabricated using the via process with Re top-electrodes have low subgap resistance and phase qubit energy relaxation time $T_1 = 15$ ns. This energy relaxation time is much smaller than the $T_1 = 500$ ns measured for a large area (49 μm^2) epitaxial $Re–Al_2O_3–Al$ phase qubit [4] fabricated using a trilayer process in the same laboratory as the devices studied in this work and also the best amorphous-barrier phase qubit with $T_1 = 600$ ns [30]. We find that our Al top-electrode devices have a high junction subgap resistance and transmon qubit energy relaxation time $T_1 =$ 500 ns. We note that the best amorphous-barrier transmon, with junction area $\sim$0.1 μm^2, has $T_1 = 2000$ ns for operation at $f \sim 6$ GHz [31].

Acknowledgments

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